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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

CEHIC, KENAN

ART UNIT

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/725,587	Applicant(s) TSUJIMOTO, HIROYUKI	
	Examiner KENAN CEHIC	Art Unit 2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 June 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 1-3, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Tetsushi (US 6,198,820).

For claim 1, Tetsushi discloses an interface device (see fig 3; 1b, 2b, 6b) for performing data transmission (see col 7 lines 5-45 “UART...transmission/receiving” and fig 3 1b-3-1 and 1b-3-2) with a further device connected coupled to a network (see fig 3; 1b and External device) at any of a plurality of transmission rates (see fig 3; Baud rate generator and col 7 lines 20-65 “set a baud rate....at a given transmission speed” and col 8 lines 1-45 “transmission speeds (600 bps and 2400 bps)” and fig 5; baud rates) that are regulated, the interface device (see fig 3) comprising:

a transmission rate control circuit (see fig 3; 1b-1 and col 7 lines 20-25 “baud rate setting register...set a baud rate (transmission speed)”) configured to generate a switch signal that changes an operation speed (see fig 3; Switching signal and col 7 lines 25- 65 “switching device...switches a frequency used according to the setting of the clock setting register” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5, External clocks used) the interface device (see

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fig 3) when the transmission rate must be switched (see col 7 lines 20-65 “baud rate setting register...set a baud rate (transmission speed)...given baud rate clock can be output” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5. Baud rates) and a clock generation circuit (see fig 3, 2b, 6b-1, 1b-2) configured to change a frequency in response to the switch signal and generate a clock signal having the changed frequency (see fig 3; Switching signal and col 7 lines 25- 67 “ switching device...switches a frequency used according to the setting of the clock setting register” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5, External clocks used).

For claim 2, Tetsushi discloses wherein the switching of the transmission rate is executed (see col 7 lines 20-65 “baud rate setting register...set a baud rate (transmission speed)...given baud rate clock can be output” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5. Baud rates) when data transmission (see col 7 lines 5-45 “UART...transmission/receiving” and fig 3 1b-3-1 and 1b-3-2) to the further device is required (see fig 3; 1b-1 and col 7 lines 20-25 “baud rate setting register...set a baud rate (transmission speed)”).

For claim 3, Tetsushi discloses wherein the transmission rate control circuit (see fig 3; 1b-1 and col 7 lines 20-25 “baud rate setting register...set a baud rate (transmission speed)”) switches to a transmission rate enabling low-speed transmission during low-speed transmission (see col 7 lines 50-65 “baud rate is 600 bps...” and col 8 lines 25-50 “transmission speeds...600bps” and fig 6, Baud Rates) and switches to a transmission rate

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enabling high-speed transmission when high-speed transmission is required (see fig 5; Baud rates see col 7 lines 50-65 “baud rate is 2400 bps...” and col 8 lines 25-50 “transmission speeds...2400 bps”).

For claim 11, Tetsushi discloses A method, comprising: configuring a transmission rate control circuit (see fig 3; 1b-1 and col 7 lines 20-57 “baud rate setting register...set a baud rate (transmission speed)”) to change operation speed (see fig 3; Switching signal and col 7 lines 25- 65 “ switching device...switches a frequency used according to the setting of the clock setting register” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5, External clocks used) of at least one of a plurality of devices (see fig 3;1b, External device) when a transmission rate must be switched (see col 7 lines 20-65 “baud rate setting register...set a baud rate (transmission speed)...given baud rate clock can be output” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5. Baud rates); and changing the operation speed (see fig 3; Switching signal and col 7 lines 25- 67 “ switching device...switches a frequency used according to the setting of the clock setting register” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5, External clocks used) of the at least one of the plurality of devices based (see fig 3;1b, External device) on the configured transmission rate control circuit (see fig 3; 1b-1 and col 7 lines 20-57 “baud rate setting register...set a baud rate (transmission speed)”),

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wherein said configuring the transmission rate control circuit includes (see fig 3; 1b-1 and col 7 lines 20-25 “baud rate setting register...set a baud rate (transmission speed)”) configuring the transmission rate control circuit (see fig 3; 1b-1 and col 7 lines 20-25 “baud rate setting register...set a baud rate (transmission speed)”) to generate a switch signal that changes an operation speed (see fig 3; Switching signal and col 7 lines 25- 65 “ switching device...switches a frequency used according to the setting of the clock setting register” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5, External clocks used) the interface device (see fig 3) when the transmission rate must be switched (see col 7 lines 20-65 “baud rate setting register...set a baud rate (transmission speed)...given baud rate clock can be output” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5. Baud rates) and configuring a clock generation circuit (see fig 3, 2b, 6b-1, 1b-2) configured to change a frequency in response to the switch signal and generate a clock signal having the changed frequency (see fig 3; Switching signal and col 7 lines 25- 67 “ switching device...switches a frequency used according to the setting of the clock setting register” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5, External clocks used).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
2. Claim 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Tetsushi (US 6,198,820) in view of Domon et al (US 6,950,408 B1).

For claim 4, Harriman et al teaches all the claimed invention as described in paragraph 3. Harriman et al does not teach switching to a low-speed transfer rate when connection is set up. Domon et al, from the same or similar field of endeavor, teaches the interface device (see Figure 1), wherein a transmission rate control circuit (see Figure 1, 41) switches to a transmission rate enabling minimum speed transmission operation (see column 8 lines 46-49 and 54-62) when starting operation for connection to the network (see column 8 lines 40-46) or when data is not being transmitted.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Harriman by using the features, as taught by Domon, in order to provide configuration data at the lowest supported speed so that all nodes in the network, which might only support the lowest speed, are configured correctly.

3. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tetsushi (US 6,198,820) in view of Cook et al (5,504,757).

For claims 5-7 Tetsushi discloses all the claimed invention as described in paragraph 3.

Tetsushi is silent about:

For claim 5, The interface device, further comprising a register for storing among the plurality of transmission rates, a transmission capacity of the interface itself, a transmission rate that is presently possible , and a transmission rate to be switched to next.

For claim 6, the interface device, wherein the register stores information) for a mode for maintaining the present transmission rate or information for a mode for switching to a transmission rate enabling the minimum speed transmission operation .

For claim 7, that the interface device, wherein setting of the operation mode stored in the register is changeable by a bus reset.

Cook from the same or similar field of endeavor discloses a serial bus system with the following features:

For claim 5, Cook et al. disclose The interface device (see column 4, lines 39-44) , further comprising a register for storing (see column 3 lines 47- 51) among the plurality of transmission rates (see column 9 lines 4-6), a transmission capacity of the interface itself (see column 10 lines 25-28), a transmission rate that is presently possible (see column 7 lines 55-58 and column 10 lines 25-28), and a transmission rate to be switched to next (see column 7 lines 60 – 64).

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For claim 6, Cook et al. discloses the interface device (see Figure 1B and column 4, lines 39-44), wherein the register stores information (see column 3 lines 47- 51) for a mode for maintaining the present transmission rate (see column 8 lines 36-39) or information for a mode for switching to a transmission rate enabling the minimum speed transmission operation (see column 8 lines 7-10).

For claim 7, Cook discloses that the interface device (see column 4, lines 39-44), wherein setting of the operation mode stored in the register (see column 3 lines 47- 51) is changeable by a bus reset (see column 1 lines 55-62)

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Tetsushi by using the features, as taught by Cook, in order to provide obtaining a transfer speed prior to each isochronous transfer rather than storing a predetermined speed (see column 2)

4. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Harriman, JR et al. (US 5,442,750) in view of Tetsushi (US 6,198,820)

For claim 8, Harriman discloses a method (see col 1, lines 49-60 “method”) for controlling (see col 5 lines 30-65 "protocol rules") an interface device (see Fig 1, 10) for performing data transmission (see col 4 lines 1-20 “subword” transmission along...bus 14”) with other devices connected (see col 5 lines 30-65 " each node connected to the sub-busall destination nodes") to a network (see Fig 1, 14, 26a-n and col 5 lines 30-65 “each node connected to the sub-bus...all destination nodes”) at any of a plurality of transmission rates (see Fig 1, 30 “SPEED selection” and see col 3 lines 35-45 “operates

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at a speed selected”) that are regulated (see Fig 1, 30, 24), the method comprising: providing the interface device (see Fig 1, 10) and each device (see col 5 lines 30-65 " each node connected to the sub-busall destination nodes") that are configured to change its own operation speed (see Fig 1, 30 "SPEED selection" and see col 3 lines 35-45 "operates at a speed selected" and col 5 lines 30-65 "transmission speed can be increased if and only if all destination nodes can read....at the higher rate....as indicated by the speed selection circuitry....."); and changing operation speeds of each device (see Fig 1, 30 "SPEED selection" and see col 3 lines 35-45 "operates at a speed selected" and col 5 lines 30-65 "transmission speed can be increased if and only if all destination nodes can read....at the higher rate") and the interface device (see Fig 1, 30 "SPEED selection" and see col 3 lines 35-45 "operates at a speed selected" and col 5 lines 30-65 "transmission speed can be increased if and only if all destination nodes can read....at the higher rate") from a low-speed transmission rate to a high-speed transmission rate (see Fig 1, 30 "SPEED selection" and see col 3 lines 35-45 "operates at a speed selected" and col 5 lines 30-65 "transmission speed can be increased if and only if all destination nodes can read....at the higher rate....highest speed") when switching to a high-speed transmission rate is required (see Fig 1, 30 "SPEED selection" and see col 3 lines 35-45 "operates at a speed selected" and col 5 lines 30-65 "transmission ...at highest speed....received information....transmission speed can be increased if and only if all destination nodes can read....at the higher rate") and each device included in a route (see Fig 1, 30 "SPEED selection" and see col 3 lines 35-45 "operates at a speed selected" and col 5 lines 30-65 "transmission speed can be increased if and only if all destination nodes

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can read....at the higher rate”) to a transmission destination (see Fig 1, 30 “SPEED selection” and see col 3 lines 35-45 “operates at a speed selected” and col 5 lines 30-65 “transmission speed can be increased if and only if all destination nodes can read....at the higher rate”) is compatible for the high-speed transmission (see Fig 1, 30 “SPEED selection” and see col 3 lines 35-45 “operates at a speed selected” and col 5 lines 30-65 “transmission speed can be increased if and only if all destination nodes can read....at the higher rate”) .

Harriman is silent about:

For claim 8, wherein the interface device includes a transmission rate control circuit and a clock generation circuit , and said changing operation speeds of each device and the interface device includes: transmission rate control circuit generating a switch signal that changes an operation speed the interface device when the transmission rate must be switched and a clock generation circuit changing a frequency in response to the switch signal and generate a clock signal having the changed frequency.

Tetsushi from the same or similar field of endeavor discloses the following:

For claim 8, Tetsushi discloses wherein the interface device includes a transmission rate control circuit (see fig 3; 1b-1 and col 7 lines 20-25 “baud rate setting register...set a baud rate (transmission speed)”) and a clock generation circuit (see fig 3, 2b, 6b-1, 1b-2):

the transmission rate control circuit (see fig 3; 1b-1 and col 7 lines 20-25 “baud rate setting register...set a baud rate (transmission speed)”) configured to generate a switch signal that changes an operation speed (see fig 3; Switching signal and col 7 lines 25- 65

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“ switching device...switches a frequency used according to the setting of the clock setting register” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5, External clocks used) the interface device (see fig 3) when the transmission rate must be switched (see col 7 lines 20-65 “baud rate setting register...set a baud rate (transmission speed)...given baud rate clock can be output” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5. Baud rates) and a clock generation circuit (see fig 3, 2b, 6b-1, 1b-2) configured to change a frequency in response to the switch signal and generate a clock signal having the changed frequency (see fig 3; Switching signal and col 7 lines 25- 67 “ switching device...switches a frequency used according to the setting of the clock setting register” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5, External clocks used).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Harriman by using the features, as taught by Tetsushi, in order to provide a power saving technique by using a lower clock frequency (see Tetsushi col 2-3, col 8 lines 25-50).

5. Claim 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Harriman, JR et al. (US 5,442,750) and Tetsushi (US 6,198,820) as applied above to claim 8, further in view of Domon et al (US 6,950,408 B1).

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For claim 9, Harriman and Tetsushi discloses all the claimed invention as described in paragraph 4.

Harriman and Tetsushi are silent about:

For claim 9, determining whether the high-speed transmission is required or not after the high-speed transmission ends ;

setting information for a mode for continuing high-speed transmission when the high-speed transmission is required, and setting information for a mode for switching to a transmission rate enabling minimum speed transmission operation when the high-speed transmission is not required.

Domon et al. from the same or similar field of endeavor, discloses a method for controlling an interface device (see Figure 1), further comprising:

determining whether the high-speed transmission is required or not (see column 6 lines 25-31) after the high-speed transmission ends (see column 6, lines 15-21, setting physical ID, sets the speed to low speed of 100 Mbps);

setting information for a mode for continuing high-speed transmission (see column 6, lines 6-12) when the high-speed transmission is required (see column 5, line 23-25), and setting information for a mode for switching to a transmission rate enabling minimum speed transmission operation (see column 6 lines 34-39) when the high-speed transmission is not required (see column 5 lines 14-18, conversion is needed when sending packets from a 400 Mbps to 100 Mbps node).

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It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Harriman and Tetsushi by using the features, as taught by Domon, in order to provide efficient bus usage, preventing wasted bandwidth

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harriman, JR et al. (US 5,442,750), Tetsushi (US 6,198,820), and Domon et al (US 6,950,408 B1) as applied to claim 9 above, further in view of Hester et al. (US 5,097,410)

For claim 10, Harriman, Tetsushi, and Domon discloses the claimed invention as described in paragraph 5.

Further for claim 10, Domon discloses individually changing the respective setting of the operation modes (see col 10 lines 45-60 “reinitiate the isochronous transfer” and col 4 lines 8-30 “isochronous packets”) of each device (see Fig 5, 101, 241) and the interface device (see Fig 5, 101, 241) itself (see col 10 lines 45-60 “reinitiate the isochronous transfer” and col 4 lines 8-30 “isochronous packets” and col 7 lines 1-10 “isochronous resource manager connected to the bus B2”) with the bus reset (see col 10 lines 45-60 “bus reset” and col 16 lines 30-35 “bus reset”).

Harriman, Tetsushi, and Domon are silent about:

For claim 10, generating a bus reset after the high-speed transmission ends.

Hester from the same or similar field of endeavor discloses a communication network with the following features:

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For claim 10, Hester discloses generating a bus reset (see col 19 lines 55-56 “bus to a reset”) after the high-speed transmission ends (see col 19 lines 55-56 “data transfer is complete”)

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Harriman, Tetsushi, and Domon by using the features, as taught by Hester, in order to minimize size by having a bi-directional data bus (see Hester col 2).

7. Claim 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Tetsushi (US 6,198,820) in view of Mitsuishi et al (US 5,774,702)

For claim 12, Tetsushi discloses an interface device (see fig 3; 1b, 2b, 6b and fig 6) comprising: an input/output port (see fig 3; 1b-3), coupled to a network (see fig 3; 1b and External device), inputting data (see fig 3; Receiving module and col 7 lines 5-45 “UART...transmission/receiving”) to another interface device (see fig 3; External Interface, External Device) or outputting the data (see fig. 3; Transmission Module and col 7 lines 5-45 “UART...transmission/receiving”) from the another interface device through the network (see fig 3; External Interface, External Device) at any of a plurality of transmission rates (see fig 3; Baud rate generator and col 7 lines 20-65 “set a baud rate....at a given transmission speed” and col 8 lines 1-45 “transmission speeds (600 bps and 2400 bps)” and fig 5; baud rates); and a transmission rate control circuit (see fig 3; 1b-1 and col 7 lines 20-25 “baud rate setting register...set a baud rate (transmission speed)”) changing an operation speed of the

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interface device (see fig 3; Switching signal and col 7 lines 25- 65 “ switching device...switches a frequency used according to the setting of the clock setting register” and col 8 lines 1-40 “switches the output signal...12.6 MHz...32.768 KHz...600bps...2400 bps...” and fig 5, External clocks used) from a low speed to a high speed in the case that a switching of the transmission rate is requested (see fig 3; 1b-1 and col 7 line 50 through col 8 line 25 "baud rate is 600bps..when the baud rate is 2400bps...in the remaining baud rates, the signal is switched over to the output signal of the high-frequency clock oscillator"); interface device (see fig 3; 1b, 2b, 6b and fig 6) operating at a high speed (see fig 3; 1b-1 and col 7 line 50 through col 8 line 25 "baud rate is 600bps..when the baud rate is 2400bps...in the remaining baud rates, the signal is switched over to the output signal of the high-frequency clock oscillator")

Tetsuhi is silent about:

For claim 12, returning an operation speed of a device from to the low speed in the case that an operating state of the device is reset.

Mitsuishi from the same or similar field of endeavor discloses a communication network with the following features:

For claim 12, Mitsuishi discloses returning an operation speed of a device from to the low speed in the case that an operating state of the device is reset.

(see col 39 lines 53-65 “reset is effected with a particular terminal at the High level....system starts on a low-speed clock signal”).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Tetsushi by using the features, as taught by Mitsuishi,

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in order to provide system/method consumes less power with respect to the system clock signal (see Mitsubishi col 1-2)

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENAN CEHIC whose telephone number is (571)270-3120. The examiner can normally be reached on Monday through Friday 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KWANG BIN YAO can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenan Cehic/
Examiner, Art Unit 2616

/Kwang B. Yao/
Supervisory Patent Examiner, Art Unit 2616